Design Considerations when Migrating between Intel's 8x930HD3 and 8x930HF0 USB Hub Controllers.

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June 10, 1997
Rev. 2.1

OBJECTIVE:

This document describes the hardware and software issues for converting from the Intel's 8x930HD3 USB hub controllers with 3 external downstream ports to the Intel's 8x930HF0 USB hub controllers with 4 external downstream ports. Customers need to perform thorough validation of their applications hardware and software after changes and prior to production. Intel assumes no liability for using the information provided by this document.

SUMMARY:

The main change from the 8x930HD3 to the 8x930HF0 is the addition of an external downstream port. This port is the fifth 8x930HF0 downstream port (or Hub Port 5) as shown in Table 1 below:

Downstream Port Number	*8x930HD3*	*8x930HF0*
1	External	External
2	External	External
3	External	External
4	Internal (Embedded Function)	Internal (Embedded Function)
5	-	External (new addition)

Table 1. 8x930Hx Downstream Ports

1. PART NAME AND TOP SIDE MARKING CHANGES

The part names will remain the same except for the last two characters at the end of the name. One example is “N80930HD3” would now be marked as shown in Figure 1 below as “N80930HF0”.

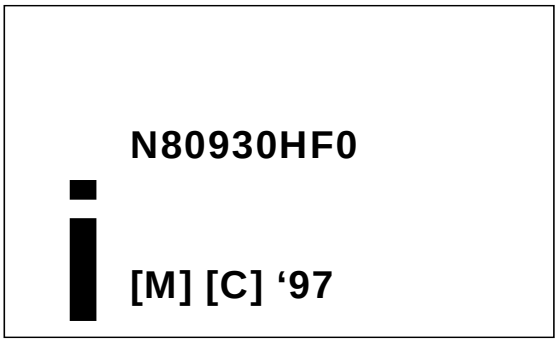

Figure 1. Example 8x930Hx0 Top Side Marking

All the available part names are shown in Table 2 below:

8x930Hx3 Part Name	*8x930Hx0 Part Name*	*RAM Size*	*ROM Size*	*Package*
N80930HD3	N80930HF0	1K Bytes	ROMless	68-pin PLCC
N83930HD3	N83930HF0	1K Bytes	8K Bytes	68-pin PLCC
N83930HE3	N83930HG0	1K Bytes	16K Bytes	68-pin PLCC
U80930HD3	U80930HF0	1K Bytes	ROMless	64-pin SDIP
U83930HD3	U83930HF0	1K Bytes	8K Bytes	64-pin SDIP
U83930HE3	U83930HG0	1K Bytes	16K Bytes	64-pin SDIP

Table 2. Available 8x930Hx Part Names

2. PINOUT CHANGES

The Table 3 and Table 4 below show the pinout differences on the 64-pin SDIP and 68-pin PLCC packages; all other pins remain the same.

Pin #	*8x930Hx3*	*8x930Hx0*
39	Reserved	DM5
40	Reserved	DP5

Table 3. 64-pin SDIP Package Pinout Differences

Pin #	*8x930Hx3*	*8x930Hx0*
59	OVRI#	DM5
60	UPWEN#	DP5
61	Reserved	OVRI#
62	Reserved	UPWEN#

Table 4. 68-pin PLCC Package Pinout Differences

3. SFR CHANGES

Two Special Function Registers (SFR) have changes:

1) **TXDAT** for Hub Endpoint 1 has added bit 5 for fifth downstream port status change report.
2) **HPPWR** for Hub has added bit 5 for fifth downstream port power enable control.

TXDAT (for Hub Endpoint 1, indexed by EPIDNEX=81h) Address: S:F3h

Bit 7	6	5	4	3	2	1	0
0	0	TXDAT.5	TXDAT.4	TXDAT.3	TXDAT.2	TXDAT.1	TXDAT.0

Mnemonic	**Function**
TXDAT.5 (new addition)	Hub port 5 status change bit
TXDAT.4:1	Hub port 1 to port 4 status change bits
TXDAT.0	Hub status change bit

Figure 2. TXDAT: Transmit FIFO Data Register

HPPWR Address: S:9Ah

Bit 7	6	5	4	3	2	1	0
-	-	HPPWR.5	HPPWR.4	HPPWR.3	HPPWR.2	HPPWR.1	-

Mnemonic	**Function**
HPPWR.5 (new addition)	Hub port 5 power enable bit
HPPWR.4:1	Hub port 1 to port 4 power enable bits

Figure 3. HPPWR: Hub Port Power Control Register

Three new SFRs have been added to support fifth downstream port control, status and status change:

1) **HPCON**
2) **HPSTAT**
3) **HPSC**

These registers can be accessed after writing a ‘05h’ to the HPINDEX register.

HPCON (for Hub Port 5, indexed by HPINDEX=05h) Address: S:CFh

Bit 7	6	5	4	3	2	1	0
0	0	-	-	-	HPCON2	HPCON1	HPCON0

Mnemonic	Function
HPCON.2:0	000 - Disable port
	001 - Enable port
	010 - Reset and enable port
	011 - Suspend port
	100 - Resume port

Figure 4. HPCON: Hub Port Control Register

HPSTAT (for Hub Port 5, indexed by HPINDEX=05h) Address: S:D7h

Bit 7	6	5	4	3	2	1	0
DPSTAT	DMSTAT	LSSTAT	PPSTAT	PRSTAT	PSSTAT	PESTAT	PCSTAT

Mnemonic	Function
DPSTAT	Dp status
DMSTAT	Dm status
LSSTAT	Low-speed device attach status
PPSTAT	Port power status
PRSTAT	Port reset status
PSSTAT	Port suspend status
PESTAT	Port enable/disable status
PCSTAT	Port connect status

Figure 5. HPSTAT: Hub Port Status Register

HPSC (for Hub Port 5, indexed by HPINDEX=05h) Address: S:D5h

Bit 7	6	5	4	3	2	1	0
-	-	-	RSTSC	-	PSSC	PESC	PCSC

Mnemonic	Function
RSTSC	Port reset status change
PSSC	Port suspend status change
PESC	Port enable/disable status change
PCSC	Port connect status change

Figure 6. HPSC: Hub Port Status Change Register

3. ROOT PORT CHANGES

The root port (Hub Port 0) of the 8x930Hx0 has been changed to only support the full speed USB edge rate (rise/fall time), since a hub must be a full speed device. The downstream ports continue to support both low and full speed USB edge rates.

As the 8x930Hx0 must be a full speed device, the PLLSEL pins configuration and the 1.5KΩ pull up on root port should remain unchanged. No hardware and software change is needed related to this.

4. UNUSED DOWNSTREAM PORTS

If the USB downstream ports are not used, it is still required that the two data pins be pulled low externally (similar to a disconnect) so that the inputs are not floated. An example of this is migrating from the 8x930Hx3 external downstream port device to the 4 external downstream port device, where the additional USB port is not being used in the application. In this case, DM5 and DP5 would still need to have 15K external pulldown resistors.

5. SPEC CHANGES

Always refer to the latest 8x930Hx Specification Updates document (order number 272962) for latest errata information and specification updates. The latest 8x930Hx Specification Updates document can be obtained from Intel FAE or Intel distributors FAE. It is also posted in the web site:

http://www.intel.com/design/usb/specupdt/